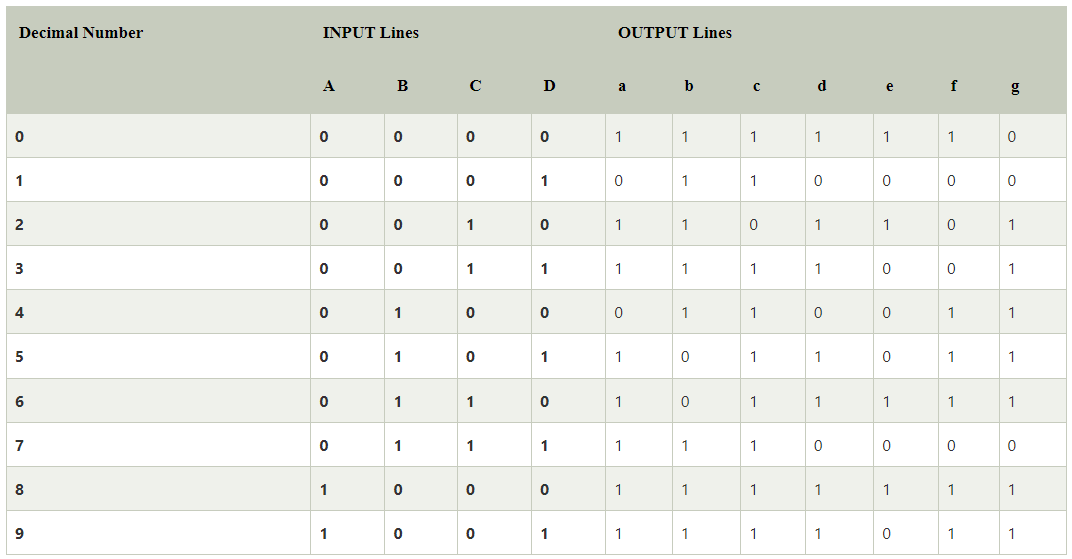
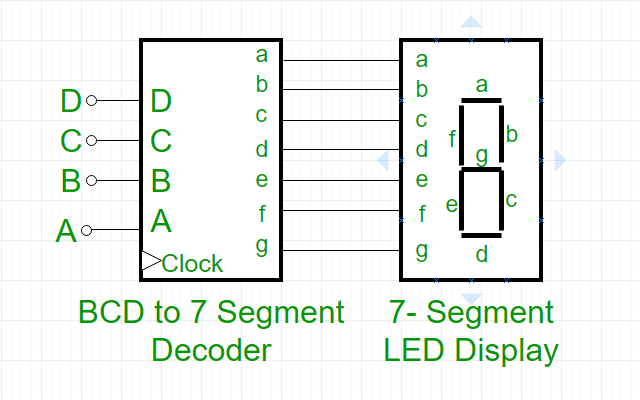
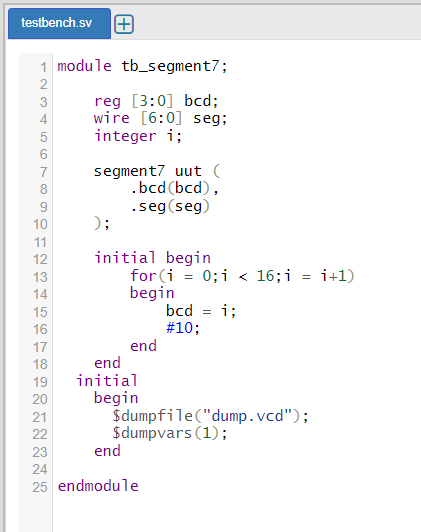
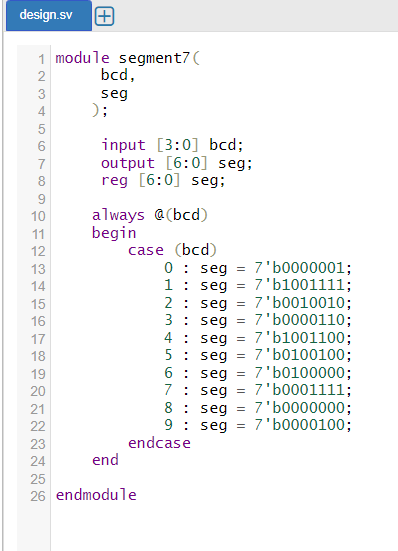
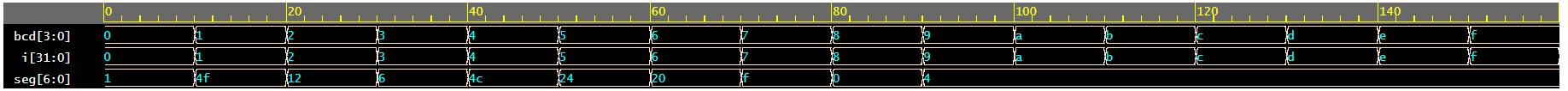
**LAB 7: Application of Decoder, Recap of Logisim**

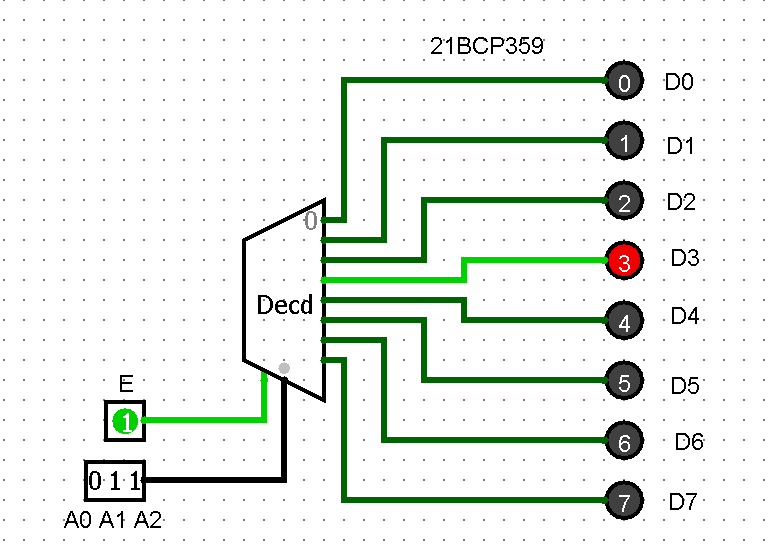
**Question 1: Write a Verilog code to implement BCD to seven segment display Decoder. Prepare the Truth Table and circuits and verify the same using Test Bench.**

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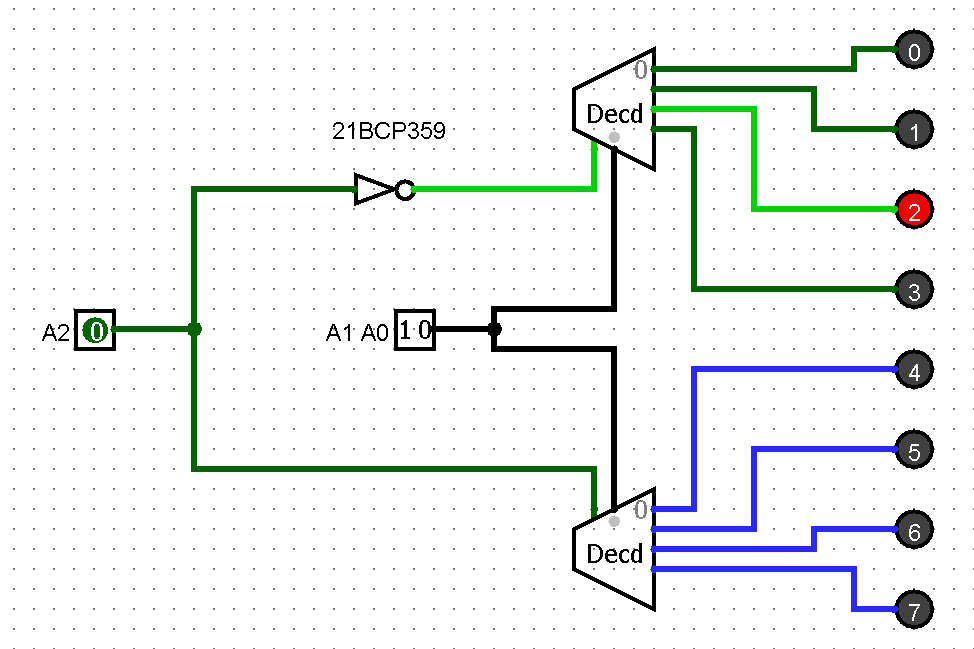
** **

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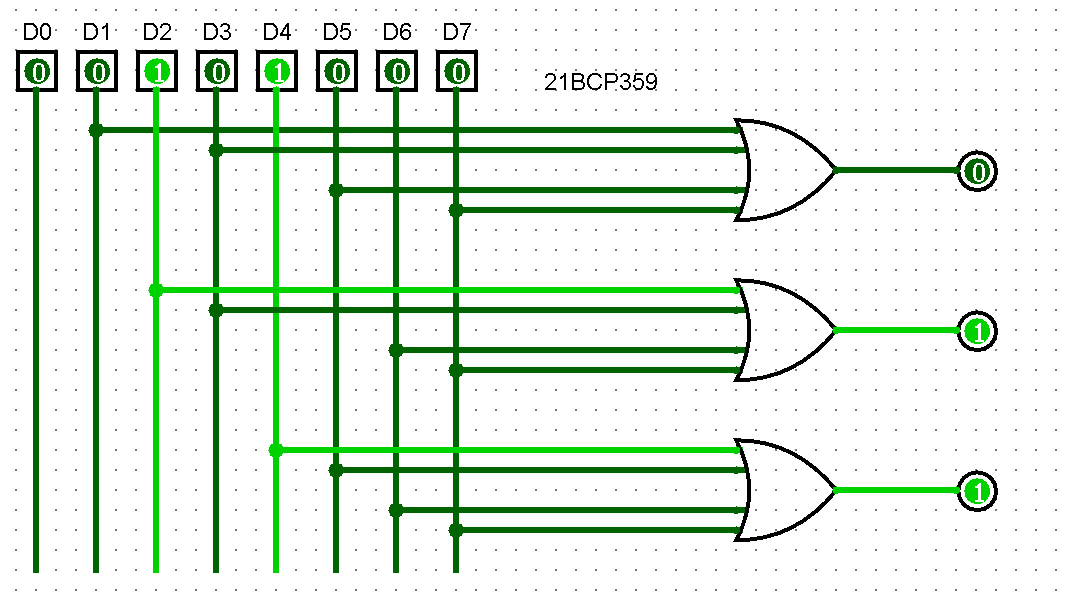
**Question 2: Design a 3:8 Decoder using Logisim.**

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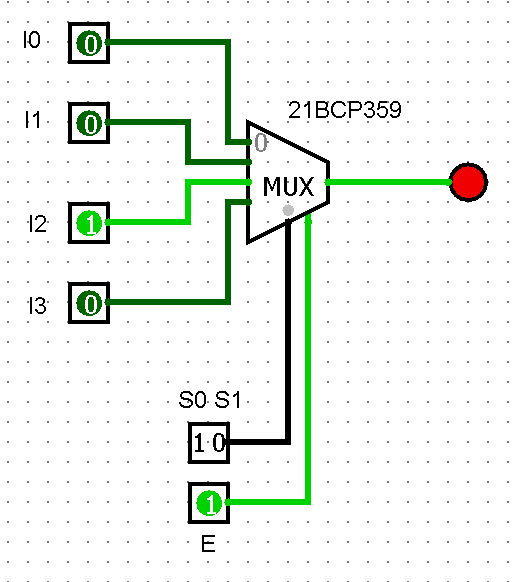
**Question 3. Design a 3:8 Decoder using two 2:4 Decoder using Logisim.**

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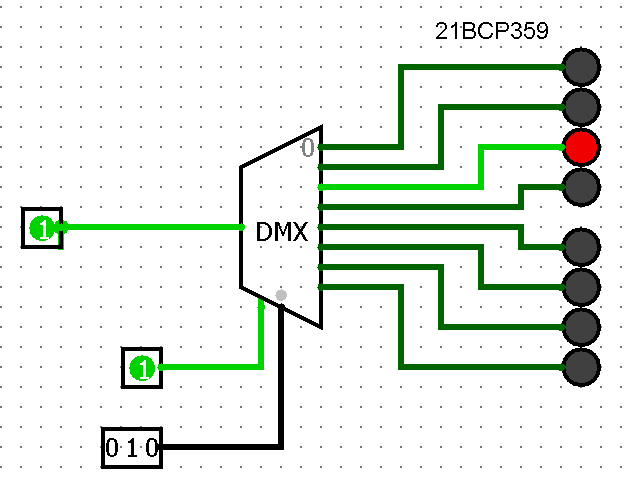
**Question 4. Design an 8:3 Priority Encoder using Logisim.**

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**Question 5. Design a 4:1 Multiplexer using Logisim.**

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**Question 6. Design a 1:8 Demultiplexer using Logisim**

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